REMARKS

By this submission accompanying with a request for continued examination, claims 7-10 are amended. Accordingly, claims 3 and 7-11 are pending in this application and are respectfully submitted for a timely examination.

Claims 8, 10 and 11 Rejected under 35 U.S.C. § 103(a)

Claims 8, 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,448,820, hereinafter "Wang") in view of the Applicants' prior art (hereinafter "APA"). To the extent it is still applicable, this rejection is respectfully traversed.

Claim 8 as amended, recites a delay time adjusting circuit for receiving a signal that is input to an input buffer comprising, among other features, a divider configured to divide a frequency of said output signal by a division rate, wherein a frequency of a signal output from said divider is less than a frequency of said input signal so as to determine how frequent a signal phase is adjusted.

Claim 10 as amended, recites a delay time adjusting method for receiving a signal that is input to an input buffer comprising, among other features, (b) dividing a frequency of said output signal by a division rate, wherein a frequency of a signal obtained by said step (b) is less than a frequency of said input signal so as to determine how frequent a signal phase is adjusted.

Claim 11 depends from independent claim 9, which recites a delay time adjusting method comprising, among other features, (a) dividing a frequency of said input signal by a first division rate so as to determine a target that is used to adjust a signal phase,

and (c) dividing a frequency of said output signal by a second division rate higher than said first division rate so as to determine how frequent the signal phase is adjusted.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Wang merely discloses a phase frequency detector (PFD) circuit (516) that compares two clock signals and generates a number of outputs to indicate a phase difference between these two clock signals (513, 519). The phase frequency detector of Wang has more than three states. The PFD circuit may be used in phase locked loop (PLL) or delay locked loop (DLL) circuit in order to maintain or lock a phase relationship between the two clock signals. The PFD circuitry will allow for a fast lock acquisition time, even when there is a relatively wide frequency range between the two clock signals.

In making the rejection, the Examiner characterized Wang as allegedly disclosing "a variable delay circuit ... in element 533 ... [and] is implemented using a number of buffers or inverters connected in a ring oscillator arrangement (column 6, lines 61-63)." The Examiner also acknowledges that "Wang does not disclose using an input buffer, an output buffer and a dummy circuit to delay a signal from the frequency divider by a fixed delay time," and relies on APA.

The Applicants submit that Wang in view of APA fails to disclose or suggest each and every element recited in claims 8, 10 and 11 of the present application. In particular, it is submitted that the cited prior art fails to disclose or suggest at least a divider configured to divide a frequency of said output signal by a division rate, wherein

a frequency of a signal output from said divider is less than a frequency of said input signal so as to determine how frequent a signal phase is adjusted, and the process of doing the same.

For instance, the Office Action acknowledges that Wang does not teach a dummy circuit to delay an output of the divider by a fixed delay time. Furthermore, the Office Action relies on the APA as teaching the dummy circuit, and asserts that it would have been obvious for those skilled in the art to incorporate the dummy circuit of the APA into the delay adjusting circuit of Wang.

However, the Applicants submit that Wang fails to teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL circuit) and a signal output from an output buffer that outputs an output signal from the PLL circuit. Further, if the signal output from the output buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels. Accordingly, it is submitted that it would not have been obvious for those skilled in the art to use a dummy circuit in Wang.

Therefore, the Applicants submit that Wang in view of APA fails to disclose each and every element recited in claims 8, 10 and 11 of the present application, and are allowable.

Accordingly, Applicants respectfully request withdrawal of the rejection.

Claims 3, 7 and 9 Rejected under 35 U.S.C. § 103(a)

Claims 3, 7 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang in view of Hanke, III et al. (U.S. Patent No. 5,376,848, hereinafter "Hanke") further in view of the APA.

Claim 7 as amended, recites a delay time adjusting circuit for receiving a signal that is input to an input buffer comprising, among other features, a first divider configured to divide a frequency of said input signal by a first division rate so as to determine a target that is used to adjust a signal phase, and a second divider configured to divide a frequency of said output signal by a second division rate higher than said first division rate so as to determine how frequent the signal phase is adjusted.

Claim 9 as amended recites a delay time adjusting method comprising, among other features, (a) dividing a frequency of said input signal by a first division rate so as to determine a target that is used to adjust a signal phase, and (c) dividing a frequency of said output signal by a second division rate higher than said first division rate so as to determine how frequent the signal phase is adjusted.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

Wang is discussed above, in which the Applicants have established that Wang fails to teach a dummy circuit. Further, as acknowledged by the Office Action, Wang fails to teach two dividers having mutually different division rates, that is, a second divider having a higher division rate than a first divider which receives the input signal.

Hanke is cited as allegedly teaching two dividers having mutually different division rates, but fails to teach or suggest a dummy circuit, and the Office Action relies on the APA as teaching a dummy circuit that is not taught in Wang nor Hanke.

However, Wang and Hanke do not teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL circuit) and a signal output from an output buffer that outputs an output signal from the PLL circuit. Further, if the signal output from the output buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels.

Hence, the Applicants submit that it would not have been obvious for those skilled in the art to incorporate the dummy circuit of the APA into the delay adjusting circuits of Wang and Hanke.

In view of the above, it is submitted that Wang in view of Hanke and further in view of APA fail to teach or suggest at least dividing a frequency of the input signal by a first division rate so as to determine a target that is used to adjust a signal phase, and dividing a frequency of the output signal by a second division rate higher than the first division rate so as to determine how frequent the signal phase is adjusted.

Accordingly, it is respectfully submitted that claims 7 and 9 are allowable over Wang, Hanke and the APA.

As claim 3 depends from claim 7, the Applicants submit that claim 3 incorporates the patentable aspects therein, and is therefore allowable for at least the reasons set

forth above with respect to the independent claim, as well as for the additional subject matter recited therein.

Accordingly, the Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 3 and 7-11 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 3 and 7-11 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to

counsel's Deposit Account No. 01-2300, referring to client-matter number 100353-00037.

Respectfully submitted,

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Enclosure: Petition for Extension of Time (three months)